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ADVANCED POWER REDUCTION TECHNIQUE FOR DRAM USING LOSSLESS COMPRESSION

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ABSTRACT

Adynamicrandom access memory(DRAM) has served as the major role in computer systems and mobile phones.In DRAMthe electrical chargeis in the form of storagecapacitorso the refreshoperationincreasesin proportiontothememorycapacity.Weproposeanewmethodto reducethem e m o r y c a p a c i t y b y u s i n g a B i t m a s s c o m p r e s s i o n t e c h n i q u e . I n t h i s t h e bitstream compression is important in reconfigurable system design since it reduces the bitstream size and the memory requirement. It also improves the communication bandwidth and thereby decreases the reconfiguration time. Existing research in this field has explored two directions: efficient compression with slow decompression or fast decompression at the cost of compression efficiency. This paper proposes a decoding compression technique to improve both compression and decompression efficiencies. The three major contributions of this paper are: 1) smart placement of compressed bitstreams that can significantly decrease the overhead of decompression engine; 2) selection of profitable parameters for bitstream compression; and 3) efficient combination of bitmask-based compression and run length encoding of repetitive patterns. Our proposed technique outperforms the existing compression approaches by 15%, while our decompression hardware for variable-length coding is capable of operating at the speed closest to the best known field-programmable gate array-based decoder for fixed-length coding.

***Index Terms*—Dynamic random access memory (DRAM),bitstream compression, variable-length coding, field-programmable gate array-based decoder**

I INTRODUCTION

Dynamicrandomaccessmemory(DRAM)hasservedasthe mainroleofstorageincomputer Systems including high perform ancesystems,personalcomputers,and mobile phones for morethan30years.Thememorycapacity ofaDRAM has increased to meetsystem demands,supported by the development ofasemi conductor process technology thatfollows Moore'slaw,wherebythenumber ofelements on afixedsilicondie doublesevery18 months.In fact,needs from the systemside have includednotonlymemory capacity, but also datatransferspeed,operation currentreduction, and standbycurrentreduction.InaDRAM, eachbitisstoredas anamountof electrical chargein a storagecapacitor,and theincreaseinmemorycapacityhasdirectlycausedtwo problems:disturbanceandpowerconsumption.

Bothoftheseproblemsareattributedtotherewriteoperationt oamemory cellassociatedwithafinitedataretentiontime. Inparticular,standbypowerconsumptionhasbecomeoneoft hemost seriousproblemsforusingaDRAM inmobileappli-cations.Followingtheconstant-electric-fieldscalingtheory, thevoltageshould belowered atthesameratebywhichthe dimensionsarereduced.Therewritevoltageis,however, saturated by the difficulty associated with thereal operation.Thismeansthatthestandbypowerincreaseswitht hememorycapacity.Anewmethodtoreducethere fresh currentinaDRAM by extending theretentiontime effectively whentheamountofthedatatobestoredissmall. We call thislow-powermode as the partial access mode (PAM).Theretentiontimehasbeenshowntoexhibitbothtaila

ndmaindistributions[6].Mostofthecellsbelongto the maindistribution andhaveretentiontimessignificantly higherthantheproductspecification. Onlyaminorportion suffersfromincreasedleakage.

Althoughtheactivepowerincreasesbyafactorof 2^N,the refresh time increases by more than 2*N* as a consequence ofthe fact that the majority decision does better than averaging for the tail distribution of retention time. The conversion can be realized very simply from the structure of the DRAM array circuit. This method can reduce the frequency of the disturbance and its power consumption by two orders of magnitude. The proposed DRAM is fully compatible with a conventional DRAM. In its usual operating mode, the full memory capacity is used. In the PAM, the capacity is limited to $2-N$ of the total capacity; however, memory cells are fully used to share the storage charge to extend the retention time.

This paper is organized as follows: in Section II, the refresh operation and retention time are explained on the basis of the measured data of the fabricated DRAM. Then, conventional methods to reduce the refresh current are examined. In Section III, we propose a PAM and describe the difference between our method and the conventional partial array self refresh method. In Section IV, we examine the distribution of the retention time of 2*N* cells/bit statistically and show that the tail distribution can be eliminated when $N \geq 2$. For 2*N*cells/bit,thecellsignalisdetermined notbytheaverage,but bythemajority ruleof 2^N cells.

TABLE IDRAMCOMPARISON

Total capacity	256-Mb	1-Gb	2-Gb
BANK structure	4BANKs	8BANKs	8BANKs
BL length	512	512	512
WL length	512	512	512
AREF	8-K	8-K	8-K
X address	X0-X12	X0-X13	X0-X14
Y address	Y0-Y9	Y0-Y9	Y0-Y9
Data	X8	X8	X8
Page size	8K	8K	8K
VDD	2.5V	1.5V	1.5V

II. DRAM OPERATION AND POWER-REDUCTION MODE

A. DRAM Refresh Operation

The DRAM memory capacity has been increasing, even though its die size has almost remained constant, as listed in Table I. In 2011, a 2-Gb DRAM was fabricated by a 30-nm [minimum feature size (F) value] process and was placed on the market. A DRAM stores a single bit in a memory cell as an amount of electrical charge on a storage capacitor. Charge is lost by the leakage current of the p-n junction, sub-threshold current, and gate-induced drain leakage (GIDL)[26]. This means that a DRAM requires a rewrite operation before the memory cell loses its storage charge. This rewrite operation is called refresh. Refresh is performed by issuing an auto-refresh command (AREF). Because refresh is a type of disturbance in the system where sense amplifier (SA) activation, pre-charging, and read or write operations are forbidden, the frequency of the AREF command should be minimized.

In this paper the refresh operation using a 256-Mb DRAM as an example is used. The refreshing of all memory cells is completed by issuing 213 = 8192 AREF commands, called an 8-K AREF operation. The data retention time of each memory cell is expressed by tret. The minimum retention time of the memory cells, tret,min, during which all memory cells maintain their own charges, should be longer than 64 ms, standardized by the cell refresh time tref [27]. Thus, the maximum time interval of an AREF command, tREF, is 64 ms/ 213 = 7.8 μs in an 8-K AREF operation.

The 256-Mb DRAM in Table I consists of four banks, each of which is composed of 16 × 16 mats. One mat is 256 kb, including 512 word-lines (WLs) and 512 bit-lines (BLs) as shown in Fig.1(a) [28], [29]. In an 8-K AREF operation, a single AREF command is accomplished by onerefresh operation for all four banks. In each bank, one refresh operation is applied to 16 mats located in the WL direction.The corresponding 16 WLs are selected at the same time, and memory node voltages are read to the BLs through transfer NMOSFETs. These signals are amplified by sense amplifiers that perform rewrite operations of an 8-K memory cells. Once an SA is activated, 16 WLs allocated on the same X address of the 16 mats in one bank are selected at once, and data are read to an 8-K BLs. This number, 8-K, is called the page size and shows the maximum data size written or read during one SA activation. If the data size for writing is greater than this page size, the system must issue a precharge command and another activate command. According to Fig. 1(a), each SA located next to the mat has common power supplies CSP for a PMOSFET and CSN for an NMOSFET: these perform pre-charging and SA amplification, as shown in Fig. 2. In the pre-charge mode, CSP, CSN, and the BL (BLT and BLB) voltages are set to VARY/2, which is half of the voltage of VARY. The high (H) and low (L) levels of the BL voltage are VARY and VSS (0 V), respectively. Initially, the SA amplification

voltage VDD is applied to BLEQB, which reduces BLT/B from VARY/2.

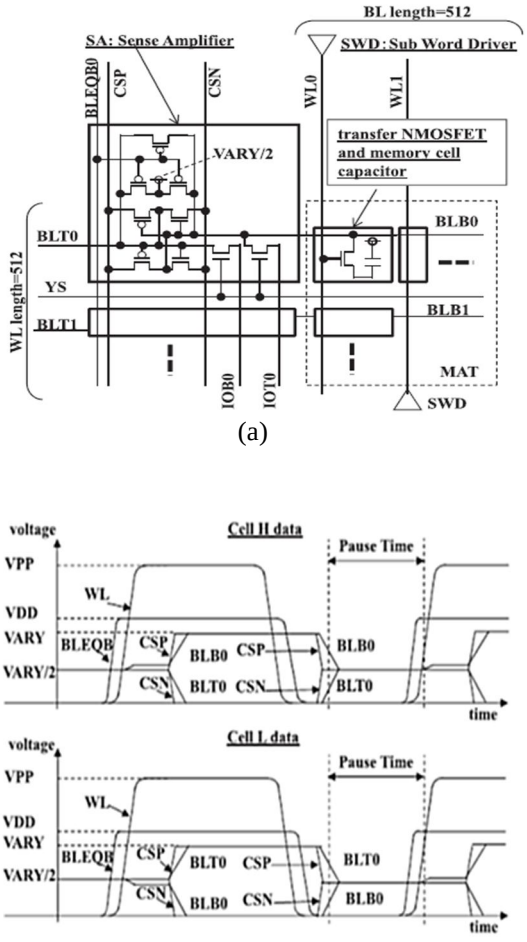


Fig. 1. (a) Array circuit and (b) its waveforms.

Then, the selection of the WL connects the memory node to the BL. The charge in the storage capacitor changes the BL voltage to a higher or lower value than VARY/2. The difference from VARY/2 is called the signal amount. After the voltage of the BL has stabilized, CSP is changed to VARY and CSN is changed to VSS at the same time. The SA increases the voltage difference between BLT and BLB to VARY. In the pre-charge mode, the WL voltage is changed to VSS to reduce the memory node from the BL voltage, and then, CSP and CSN are reduced from VARY and VSS, respectively. Finally, BLEQB is lowered to set CSP, CSN, and the BL voltage to VARY/2. Memory cell structure and leakage current path. Measured error ratio including temperature dependency. The results show zero fail bits at 100 ms and eight fail bits at 150 ms for T = 85 ◦C, which indicates 100 ms<*t*ret, min <150 ms.

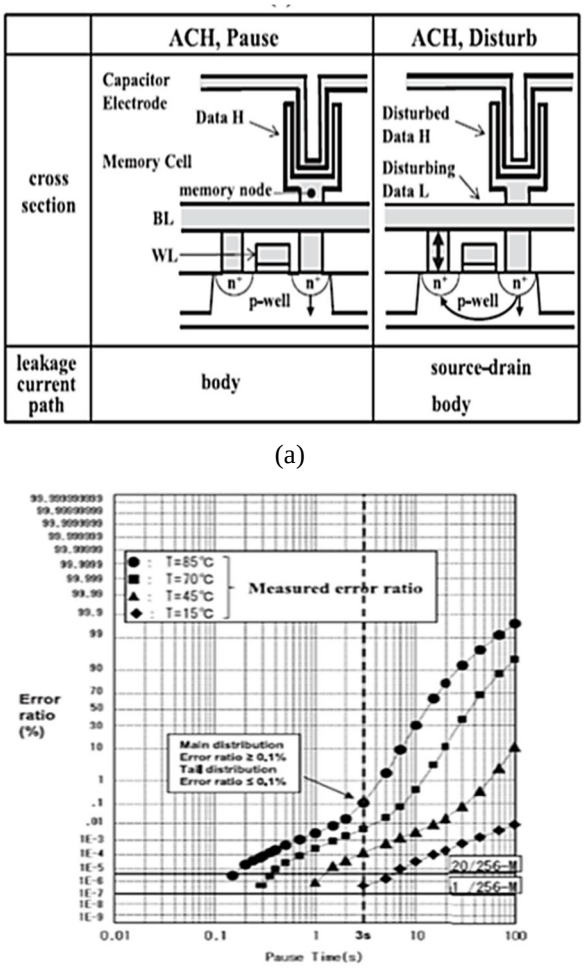


Fig. 2. (a) Memory cell structure and leakage current path. (b) Measured error ratio including temperature dependency. The results show zero fail bits
at 100 ms and eight fail bits at 150 ms for T = 85 ◦C, which indicates 100 ms<*t*ret,min<150 ms.

B. Charge Retention Time of the Storage Capacitor

The AREF interval time, *t*REF, should be as long as possibleto meet the system requirements. The user usually sets thistime to 7.8 *μ*s, which is the maximum value defined from thespecification, *t*ref of 64 ms. The retention time *t*ret dependson the characteristics of a memory cell that has a leakagecurrent that reduces the charge on the storage capacitor. Thisleakage current is caused by the diffusion and generationof electrons and holes at the p-n junction in the siliconsubstrate, the sub-threshold current, and GIDL [1], [3], and [4]. Fig. 2(a)shows the structure of the storage capacitor andtransfer NMOSFET in a memory cell. The leakage current isinfluenced by the voltages of the WL, BL, and body (p-well).This causes a variety of *t*ret values among several conditions [4], [14], and [15] . There are two states that hold the storage charge in the memory cell, described as follows.

1). The observed memory cell is not selected, and all memory cells in the same mat are not selected. WL voltage = VSS, and BL voltage = VARY/2. If the memory node voltage is H in the observed memory cell, leakage current flows from the memory node to the body [2], [3], [7], and [8]. The left panel in Fig. 2(a)shows this state. The memory node voltage H is changed to L in tret , which is the specific finite time of the cell. We call this destruction mode as the all cell high (ACH) pause. All in ACH means that the memory node voltages in all DRAM memory cells are H at the last restore time. If the memory node voltage is L, there is no destruction to H as the voltage of the body is the same voltage, L.

2). The observed memory cell is not selected, and one of the other WLs in the same mat is selected. WL voltage = VSS, and BL voltage = H or L. If the memory node voltage is H and BL voltage is L, leakage current flows not only into the body, but also into the BL. The electric field induces a current into the BL. This destruction mode is called ACH disturb. If the memory node voltage is L and BL voltage is H, only leakage current into the BL appears and there is no current into the body. This is called all cell low disturb. The case of ACH disturb is the worst because there are two current paths [2], [3], and [7]. The right panel in Fig. 2(a) shows this state.

Themeasured t_{ret} datainstate1isobtained fromthetime whenthefail-bitjudgmentofthereadcommandappearsafter apausetimeintheprechargemodefromthewriteoperation ofmemorynodevoltageH.Fig.1(b)showsthepausetime. Fora256-MbDRAM,thefail-bitcountofACHpausedenotes thenumber ofcellsofsignalLin256Mbafterthewrite operationof H. In Fig. 1(b), 1cell/bit measurementdata showthe errorratio of the 256-MbDRAMfrom100msto100s,wheretheerrorratioisdefined bythenumberof failbitsdividedby256Mb.Theerrorratioisconvertedwith aninversecumulative distributionfunctiontocheckwhether the distribution coincides withastandardnormaldistribution.

Ifthedistributionappearsasastandardnormaldistribution, thelinebecomesstraight[5],[6]. Fig. 2(b)showsthat alllines haveakinkindicating theexistenceoftwokindsofstandard normaldistributions,tailandmaindistributions.Thevariation oft_{ret}isgreaterthanthreeordersofmagnitudeatatemperature of 85°C,and t_{ret} has one orderof variationin the area whoseerrorratioislessthan0.1%.Thismeansthat,although t_{ret} of99.9%for256Mbislongerthan3s,$t_{ret,min}$ofthe 256-MbDRAMis100ms.Thisdifferenceiscausedbythetail distribution,whoseerrorratioislessthan0.1%.Furthermore, thevariationamongtemperatures isverylarge.Accordingto Fig.2(b),$t_{ret,min}$of100msatatemperature of85°C,which istheworstvalue,isimprovedto1sat45°C.IntheDRAM specification, t_{ref} ensuresat$t_{ret,min}$of64msattemperatures between0°Cand85°C[9],[10],[14],[24],and[25].A DRAMsuppliercanreplacetheworst20or30memory cells withother goodones preparedinadvance.Fig.2(b)showsthe effectof20-bitsreplacement.

C.DRAMStandbyCurrent

A DRAM consumes standby power, mainly by refresh, even when there are no read and write accesses to memory cells. The storage capacitor needs around 20 fF, independent of F, as *t*ref is always 64 ms through all generations. If the minimum feature size is cut in half by process improvement, the memory capacity of the DRAM for the same die size increases by a factor of four. The voltage to rewrite data should be lowered to maintain the same power consumption. The BL rewrite voltage VARY, however, saturates at around 1 V caused by real operation difficulties. Table I shows the external voltage saturation that is caused by SA amplification where VARY is the source voltage. Therefore, the amount of refresh current increases by a factor of four as well. In fact, the total refresh current is less than this because the other currents used to drive signals for the refresh operation become less than half owing to the miniaturization. Considering this factor, the standby power increases in every generation.

If there is no access to the DRAM, *t*ret is determined only by ACH pause 1 without disturb 2 discussed in the previous section. The DRAM has a SELF mode in the specification, which means that the DRAM performs a refresh operation by itself in the longer interval *t*ref,ctl. The oscillator circuit in the DRAM can adjust the period for *t*REF in the SELF mode. This adjustment based on the measurement of the manufactured DRAM enables a greater reduction in power consumption in the SELF mode. This *t*REF adjustment is set on the basis of the *t*ret-measured DRAM data that were compiled during the manufacturing process of the silicon wafer. If it is known in advance that the system has no access to the DRAM in a certain interval, a user issues a SELF ENTRY command, which is the longest time interval during which storage charge is not lost. Once the DRAM receives a SELF ENTRY command, it remains in the SELF mode until receiving a SELF EXIT command, and it accepts no commands except SELF EXIT [11]-[13], [16].

III. PARTIALACCESSMODE

A.ConventionalPAMMethod

Mismatches between the AREF operation in the normal mode and the preserved bank data in the PASR have been explained. Our proposed PAM eliminates these mismatches and uses all memory cells efficiently. One characteristic ofthe PAM is that it holds data using 2*N*

cells/bit to extend *t*ret. Another characteristic is the control method between 1 and 2*N*cells/bit that is located higher in the hierarchy than the control of the normal and SELF modes. The PAM reduces the refreshoperation frequency for both the normal and SELF modes. Therefore, the AREF command frequency in the normal modeand power consumption in the SELF mode are reduced at once. In contrast, the PASR reduces the power consumption in theSELF mode only.

A PAM ENTRY operation indicates a conversion from 1 to 2*N* cells/bit. This is simply a copy operation from the memory cell connected with one WL to 2*N*−1 memory cells connected with 2*N* − 1 WLs in the same mat. Table II shows how thisoperation is simply achieved by the DRAM array architecture in Fig. 1(a). This operation is performed by only a delayed WL selection. A PAM ENTRY operation is completed through 8-K/2*N* copy operations applied to all memory cells in the 256-Mb DRAM.

B. Bitmask Selection

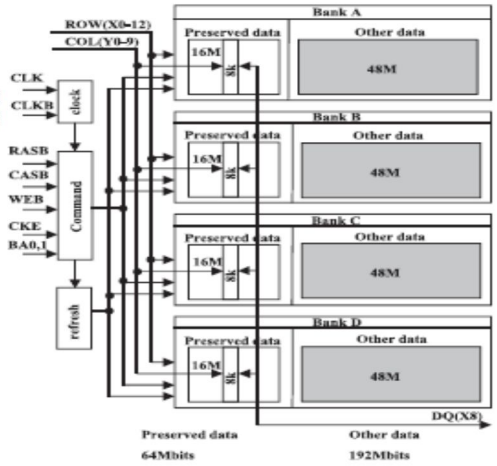
The generic encoding formats of bitmask-based compression technique for various number of bitmasks. A compressed data stores information regarding the bitmask type, bitmask location, and the mask pattern itself. The bitmask can be applied on different places on a vector and the number of bits required for indicating the position varies depending on the bitmask type.

Fig 3.(a) Block diagram for the PAM

	Bits2-0	Access Array	t_{ref}	*times*	t_{REF}
PAM	000	256M(All Banks)	64ms	8Kref	7.8μs
	001	128M(X0=0)	128ms	4Kref	31.3μs
	010	64M(X0=X1=0)	256ms	2Kref	125μs
	011	restriction	–	–	–
	100	restriction	–	–	–
	101	32M(X0=X1=X2=0)	512ms	1Kref	500μs
	110	16M(X0=X1=X2=X3=0)	1024ms	512ref	2000μs
	111	restriction	–	–	–

Fig 3(b) Specification of the PAM.

For instance, if we consider a 32-bit vector, an 8-bit mask applied on only byte boundaries requires 2-bits, since it can be applied on four locations. If we do not restrict the placement of the bitmask, it will require 5 bits to indicate any startingposition on a 32-bit vector. Bitmasks may be sliding or fixed. Fixed bitmasks are referred with the letter while sliding bitmasks are referred with the letter . For example, refers to a sliding bitmask of length 2 while refers to a fixed bitmask of length 2. A fixed bitmask is one which can be applied to fixed locations, such as byteboundaries. However, sliding bitmasks can be applied anywhere in the test vector. Since the fixed bitmasks can be applied only to fixed locations, the number of positions where they can be applied is significantly less compared to sliding bitmasks. Hence, the number of bits needed to represent them are less than sliding bitmasks.



IV. PROPOSED METHOD

A. Compressed Technique.

The compression technique used is theBitstream compression which is important in reconfigurable system design since it reduces the bitstream size and the memory requirement. It also improves the communication bandwidth and thereby decreases the reconfiguration time. This technique givesthe good compression ratio due to complex and variable-length coding.

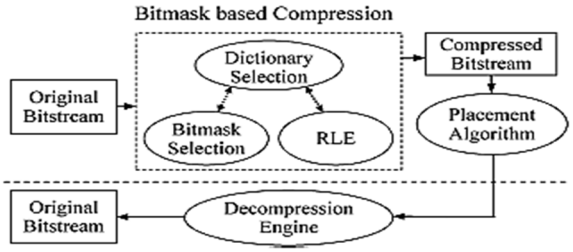
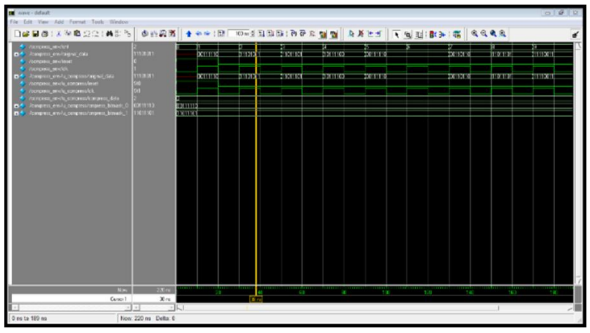


Fig. 4(a) Block diagram for Bitmask compression.

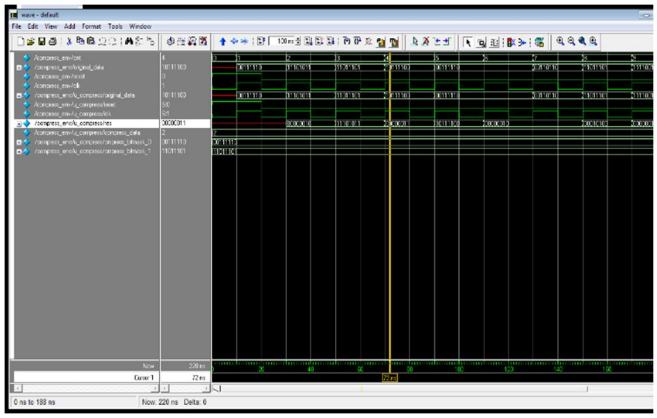
This approaches accelerate decompression using simple or fixed-length coding (FLC) where more LUTs are needed because of dictionary selection method. Fig 5(a) performs smart placement of compressed bitstreams to enable fast decompression of variable-length coding whichselects bitmask-based compression parameters suitable for bitstream compression.Finally,It efficiently combines run length encoding and bitmask-based compression to obtain better compression and faster decompression.

B. Result

The given input test vector00111110, 11101011, 11011101, 10111100, 00111110, 00111110, 00110110, 11011101, 11110011, 11011111.



The Compressed Data's are 010, 111101011, 011, 110111100, 010, 010, 0010100, 011, 111110011, 111011111.



V. CONCLUSION

The specification ofthePAMshowsthereductionof refreshoperationfrequency, whichcontributestothecurrent reduction.Inthenormalmode,thePAMisusefulift_{ACT} islongerthan260ns,eveninsituations suchascontinuous addressing. Weexaminedthet_{ret} extensionusingthefail-bitdata ofthe fabricatedDRAM.Animportantresultisthattheamountof t_{ret}extensionisnotproportionaltothecomposedcellnumber. Partialaccessconversiondoesnotcauseaparallelshiftinthe t_{ret} distribution, butdoesreducethet_{ret} variance.Thismeans thatthewidthofthet_{ret} variationapproaches zerowithan increasingnumberofcomposedcells,whichisoneexample ofthelawoflargenumbers.

This paper presented the advantages of bitmask-based compression. This paper developed efficientbitmask for test data compression in order to create maximum matching patterns. Our test compression technique used the bitmask selection methods to significantly reduce the testing time and memory requirements.

Our proposed technique outperforms the existing compression approaches by 15%, while our decompression hardware for variable-length coding is capable of operating at the speed closest to the best known field-programmable gate array-based decoder for fixed-length coding.

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